ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device is provided in which current consumption is reduced at the time a data access by consecutive addresses is performed to a ROM circuit or a RAM circuit. The semiconductor integrated circuit device incorporates a ROM circuit 1 and a control circuit 68 for controlling a data access to the ROM circuit, wherein an address generation circuit 69 included in the control circuit divides a clock to be input, performs a phase adjustment by sampling the divided clock and generates an address signal of several bits in which only a value of 1 bit changes in a sequential order when a data access by consecutive addresses is performed on the ROM circuit.